CLAIMS

1. A switching network for switching frames of data, in defined time-slots, of a cross-connection request between a desired input and a desired output, comprising an input stage consisting of a plurality of switching matrices, an intermediate stage consisting of a plurality of switching matrices, and an output stage consisting of a plurality of switching matrices, each input stage switching matrix having a link to each intermediate stage switching matrix and each intermediate stage switching matrix having a link to each output stage switching matrix, including means for routing each time-slot of each frame independently through the switching matrices.

2. A switching network as claimed in claim 1, in which the routing means is arranged to route each succeeding time-slot of the cross-connection request frame through the intermediate stage switching matrix having the link with the largest instantaneous number of free time-slots.

3. A switching network as claimed in claim 2, in which the links are between the intermediate stage switching matrix and the output stage switching matrix of the requested output.

4. A switching matrix as claimed in claim 3, in which the routing means is arranged to route each succeeding time-slot through the intermediate stage switching matrix having the link from the input stage switching matrix at which the request was received with the largest instantaneous number of free time-slots, in the event that a plurality of

intermediate stage switching matrices have equal instantaneous numbers of free time-slots in the links to the output stage switching matrices.

5. A switching matrix as claimed in any one of claims 1 to 4, in which the routing means is arranged to create a list of free time-slots in the links between the intermediate stage switching matrices and the input and output stage switching matrices of the request when a cross-connection request is received.

6. A switching matrix as claimed in any one of claims 1 to 5, in which the links are time division multiplex links.

7. A switching matrix as claimed in any one of claims 1 to 6, in which the number of intermediate stage switching matrices is at least two less than the sum of the number of inputs of each input stage switching matrix and outputs of each output stage switching matrix.

8. A switching matrix as claimed in any one of claims 1 to 6, in which the number of intermediate stage switching matrices is less than twice the number of inputs of each input stage switching matrix.

9. A switching matrix as claimed in claim 8, in which the number of intermediate stage switching matrices is less than one and one half times the number of inputs of each input stage switching matrix.

10. A switching matrix as claimed in any one of claims 1 to 9, in which the routing means is arranged to re-assemble the individually-routed time-slots into frames at the output of the output stage switching means.

11. A switching matrix as claimed in any one of claims 1 to 10, in which the switching means is adapted to receive standard data traffic from which internally-generated frames replacing at least some overhead have been created.

12. A switching matrix as claimed in any one of claims 1 to 11, in which each time-slot of the links corresponds to a frame having a data rate at least one sixteenth of that of the links.

13. A switching matrix as claimed in claim 12, in which the time-slots can each accommodate an AU-3 frame of the SDH standard.

14. A digital cross-connect, including a switching matrix as claimed in any one of claims 1 to 13.

15. A method of routing frames of data in defined time-slots through a switching network to fulfil a cross-connection request between a desired input and a desired output, wherein the switching network comprises an input stage consisting of a plurality of switching matrices, an intermediate stage consisting of a plurality of switching matrices, and an output stage consisting of a plurality of switching matrices, each input

stage switching matrix having a link to each intermediate stage switching matrix and each intermediate stage switching matrix having a link to each output stage switching matrix, the method including the step of routing each time-slot of each frame independently through the switching matrices.

16. A method as claimed in claim 15, in which each succeeding time-slot of the cross-connection request frame is routed through the intermediate stage switching matrix having the link with the largest instantaneous number of free time-slots.

17. A method as claimed in claim 16, in which the links are between the intermediate stage switching matrix and the output stage switching matrix of the requested output.

18. A method as claimed in claim 17, in which each succeeding time-slot is routed through the intermediate stage switching matrix having the link from the input stage switching matrix at which the request was received with the largest instantaneous number of free time-slots, in the event that a plurality of intermediate stage switching matrices have equal instantaneous numbers of free time-slots in the links to the output stage switching matrices.

19. A method as claimed in any one of claims 15 to 18, in which there is created a list of free time-slots in the links between the intermediate stage switching matrices and the input and output stage switching matrices of the request when a cross-connection request is received